



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Herbert Taucher et al

Art Unit: 2133

Serial No.: 10/670,567

Examiner: To be assigned

Filing Date: 09/26/2003

Docket No.: 2002P1528US

For: Method and device for testing the mapping/implementation of a model of a logic circuit onto/in a hardware emulator

Assistant Commissioner for Patents  
Office of Initial Patent Examination  
Customer Service Center  
United States Patent & Trademark Office  
2011 South Clark Place  
Customer Window, Mail Stop Application Number  
Crystal Plaza Two, Lobby, Room 1B03  
Arlington, Virginia 22202 USA

**REQUEST FOR CORRECTED FILING RECEIPT**

Dear Sir or Madam:

Via DHL, Pages 3

Applicant hereby requests that a corrected Updated Filing Receipt be issued in the above-identified patent application. The official Filing Receipt received by Applicant, a copy of which is attached hereto, has the following inaccuracies appearing thereon as indicated by quotation marks and herein requested corrections for which are indicated by double dashes:

1. Please add the complete address of the first Applicant:

-- Herbert Taucher, Wiener Strasse 9/5, A-2340 Moedling --  
and

2. Please add the names of the second and third Applicants:

-- Karlheinz Krause, Rudolfstrasse 92, D-82152 Planegg --  
and

-- Majid Ghameshlu, Kopalgasse 40/10, A-1110 Wien --.

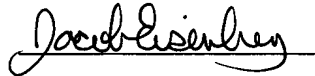
The Patent and Trademark Office is invited to contact the undersigned for any reason which would expedite the handling of this matter. In the event that the Patent and Trademark Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No.: 502464** referencing docket no.: 2002P15288US. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Date: 01-07-2004

Siemens Schweiz  
I-44 Intellectual Property  
Albisriederstrasse 245  
Zurich, CH-8047 Switzerland

**Enclosures:**  
- Official Filing Receipt (copy)

Respectfully submitted,



Jacob Eisenberg  
Attorney for Applicant  
Registration Number 43,410  
**CUSTOMER NUMBER: 28204**



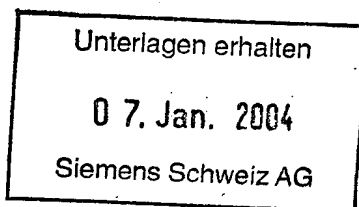
## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1459  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov

APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/670,567	09/26/2003	2133	750	2002P15288US	1	9	2

CONFIRMATION NO. 2326

28204  
 SIEMENS SCHWEIZ  
 I-44, INTELLECTUAL PROPERTY  
 ALBISRIEDERSTRASSE 245  
 ZURICH, CH-8047  
 SWITZERLAND



## FILING RECEIPT



\*OC000000011517956\*

Date Mailed: 12/17/2003

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

## Applicant(s)

Herbert Taucher, Residence Not Provided;

## Domestic Priority data as claimed by applicant

## Foreign Applications

If Required, Foreign Filing License Granted: 12/17/2003.

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

## Title

Method and device for testing the mapping/implementation of a model of a logic circuit onto/in a hardware emulator

## Preliminary Class